INTERRUPT REQUEST CONTROLLER

Abstract of the Disclosure

An interrupt request controller for processing a plurality of interrupt logic signals. The controller includes: a programmable bit masking section fed by the interrupt logic signals, adapted to mask selected ones of the interrupt signals; a interrupt priority section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined priority criteria. The request controller includes: a programmable section fed by the interrupt signals, for selecting assertion sense and/or assertion type of each one of the interrupt signals. The programmable section stores a bit for each one of the interrupt logic signals representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted and for producing a corresponding output logic interrupt signal in accordance therewith. The programmable section stores a bit for each one of the interrupt logic signals representative of whether the logic state of the interrupt logic signal should remain as an edge or be converted to a level and for producing a corresponding output logic interrupt signal in accordance therewith.